UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/750,523	12/31/2003	Kimming So	15057US02	1971

23446 7590 06/16/2006

MCANDREWS HELD & MALLOY, LTD
500 WEST MADISON STREET
SUITE 3400
CHICAGO, IL 60661

EXAMINER	
CAMPOS, YAIMA	

ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 06/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/750,523	SO ET AL.	
	Examiner	Art Unit	
	Yaima Campos	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 December 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/8/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The instant application having Application No. 10/750,523 has a total of 20 claims pending in the application; there are 4 independent claims and 16 dependent claims, all of which are ready for examination by the examiner.

I. INFORMATION CONCERNING OATH/DECLARATION

Oath/Declaration

2. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in **37 C.F.R. 1.63.**

II. STATUS OF CLAIM FOR PRIORITY IN THE APPLICATION

As required bye **M.P.E.P. 201.14(c)**, acknowledgement is made of applicant's claim for priority based on application filed on 7/15/03 (Provisional 60/487425).

III. INFORMATION CONCERNING DRAWINGS

Drawings

3. The drawings are objected to because of the following reasons:

Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified

and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

IV. ACKNOWLEDGEMENT OF REFERENCES CITED BY APPLICANT

4. The information disclosure statement filed June 8, 2004 fails to comply with the provisions of 37 CFR 1.97, 1.98 and MPEP § 609 because:

Applicant is citing an entire textbook without pointing out the specific sections and their relevance. Applicant might consider providing a new Information Disclosure Statement referring to specific sections of the cited reference with a concise explanation of their relevance.

It has been placed in the application file, but the information referred to therein has not been considered as to the merits. Applicant is advised that the date of any re-submission of any item of information contained in this information disclosure statement or the submission of any missing element(s) will be the date of submission for purposes of determining compliance with the requirements based on the time of filing the statement, including all certification requirements for statements under 37 CFR 1.97(e). See MPEP § 609.05(a).

V. OBJECTIONS TO THE SPECIFICATION

Claim Objections

5. **Claim 4, 11 and 19** are objected to because of the following informalities:

6. As per **claims 4 and 11,** the word "MIPS" should be defined within the scope of the claims. Applicant might consider amending this claims to substitute this word by – **Million Instructions Per Second (MIPS)-**.

7. As per **claim 19**, the term "TLB" should be defined within the scope of this claim. Applicant might consider amending this claim to substitute this term by –**translation lookaside buffer (TLB)-** or adding the term –**(TLB)-** in claim 18, line 3 after the first occurrence of the phrase "translation lookaside buffer."

8. Appropriate correction is required.

VI. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. **Claims 1-2, 6, 12-13 and 15-19** are rejected under 35 U.S.C. 102(b) as being anticipated by Hinton et al. (US 5,500,948).

11. As per **claims 1, 12, 16 and 18**, Hinton discloses a method/system "of reducing the size of a translation lookaside buffer comprising utilizing a bit obtained from a virtual page number of a virtual address for the purposes of writing and reading even and odd page frame numbers into a single page frame number field of said translation lookaside

buffer" as **["Translation Lookaside Buffer, TLB (11)" (Column 3, lines 23-25; Figure 1) and "Mini-TLB (TWB)," defined as "A small 3-entry instruction mini TLB (6)" (Columns 5-6, lines 62-67 and 1-5) to provide access to memory wherein "the instruction pointer is comprised of logical address bits including upper order bits, lower order bits, and a single bit having a first value or a second value, the single bit providing for translation of even-number pages for which the single bit has a first value and for odd-number pages for which the single bit has the second value" (Columns 1-2, lines 64-67 and 1-29; Column 6, lines 37-63; Figure 3)]**.

12. As per **claim 2 and 13**, Hinton discloses "The method of claims 1 and 12" **[See rejection to claims 1 and 12 above]** "wherein said bit corresponds to the least significant bit of said virtual page number" **[Hinton discloses this limitation as "A logical address (81) is separated into three parts. Bits 0 through 11 are an offset within an instruction page" and explains that "bit 12 selects which of the two entries in the TWB (62) are to be used for this address" (Column 6, lines 37-63; Figure 3)]**.

13. As per **claim 6**, Hinton discloses "The method of claim 1" **[See rejection to claim 1 above]** "wherein said virtual address comprises 32 bits" **[Hinton discloses this limitation as "A logical address (81) is separated into three parts. Bits 0 through 11 are an offset within an instruction page" and explains that "bit 12 selects which of the two entries in the TWB (62) are to be used for this address. Bits 13 through 31 are compared against the stored logical address in the TWB" (Column 6, lines 38-43)]**.

14. As per **claims 15, 17 and 19**, Hinton discloses the method/system of claims 12, 16 and 18 **[See rejection to claims 12, 16 above and rejection to claim 20 bellow]**

wherein said consolidating even and odd page frame numbers into a single page frame number field implements a translation lookaside buffer of reduced size **[With respect to this limitation, Hinton discloses "Translation Lookaside Buffer, TLB (11)" (Column 3, lines 23-25; Figure 1) and "Mini-TLB (TWB)," defined as "A small 3-entry instruction mini TLB (6)" (Columns 5-6, lines 62-67 and 1-5). Applicant should note that by using "a single bit having a first value or a second value, the single bit providing for translation of even-number pages for which the single bit has a first value and for odd-number pages for which the single bit has the second value" (Columns 1-2, lines 64-67), Hinton is implementing a TLB of reduced size as compared with Applicant's described prior art (Background of Applicant's Specification)]**.

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. **Claim 3, 5, 10, 14 and 20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hinton et al. (US 5,500,948).

17. As per **claims 3, 5, 10, 14 and 20**, Hinton discloses the method/system of claims 1, 12 and 19 **[(See rejection to claims 1, 12 and 19 above). Hinton also discloses using a translation lookaside buffer (TLB) for translating of instruction pointers from**

logical address to physical address (Column 3, lines 23-25) wherein instructions are "fetched from memory, instruction queues, (52) for temporary instruction storage between memory and the cache, instruction pre-decode (54) and post-decode logic (58), address translation logic (62), cache tag logic (60), and the necessary IFU control logic" (Column 3, lines 57-62) and explains that wherein memory may be external (Column 3, line 49); therefore, any kind of instructions may be used]. Hinton does not disclose expressly "wherein said reading and writing is performed by way of using an existing translation lookaside buffer (TLB) control processor instruction set" and "wherein said translation lookaside buffer of reduced size is compatible with one or more legacy systems utilizing any existing TLB instructions, software, or commands".

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use an existing translation lookaside buffer control instruction set and make the translation lookaside buffer as taught by Hinton compatible with existing TLB instructions, software, or commands as one of ordinary skill in the art would have been motivated to select from off the shelf processors at least to reduce cost and take advantage of existing system components. Furthermore, A recitation directed to the manner in which a claim is intended to be used does not distinguish the claim from the prior art if prior art has the capability to do so (See MPEP 2114 and Ex Parte Masham, 2 USPQ2d 1647 (1987).

18. As per **claims 4 and 11**, Hinton discloses "The method of claims 3 and 1" **[See rejection to claims 3 and 1 above]**; however, Hinton does not disclose expressly that "said TLB control processor instruction set comprises a MIPS control processor instruction set."

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use an instruction set which comprises a MIPS (Millions Instructions Per Second) processor instruction set which is a well-known processor type. One of ordinary skill in the art would have been motivated to select from off the shelf processors at least to reduce cost and take advantage of existing system component designs.

19. **Claim 7** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hinton et al. (US 5,500,948) in view of Bryg et al. (US 6,430,670).

20. As per **claim 7**, Hinton discloses "The method of claim 6" **[See rejection to claim 6 above]** but does not disclose expressly that "said virtual page number is defined by bits [31:12] of said 32 bit virtual address."

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to **[define a virtual page number by bits [31:12] or any other bit positions of said 32 bit virtual address]**. Applicant has not disclosed that **[defining a virtual page number within specific bit positions of a virtual address]** provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with **[a virtual page number defined as bits 13-31 as taught by Hinton]** because **[positions of a virtual page number bits vary depending on the page size used in the virtual mapping and are system-specific as taught by Bryg (Column 4, lines 9-20)]**.

21. **Claims 8-9** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hinton et al. (US 5,500,948) in view of Riedlinger et al. (US 6,446,187).

22. As per **claims 8-9**, Hinton discloses "The method of claim 6" **[See rejection to claim 6 above]**; however, Hinton does not discloses "wherein said virtual address utilizes a page mask size ranging from 4 kilobytes to 16 megabytes" or "wherein said page mask size comprises 4 kilobytes."

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to **[use a page mask of any size, including a page mask that ranges from 4 kilobytes to 16 megabytes or that comprises 4 kilobytes for virtual to physical address mapping, such as the system taught by Hinton]**. Applicant has not disclosed that **[having a virtual address utilize a page mask ranging from 4 kilobytes to 16 megabytes or a page mask of 4 kilobytes]** provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with **[any size of page mask]** because **[it is well known in art that a page mask is used to select a virtual page size (See Riedlinger, Column 4, lines 14-23)]**.

VII. RELEVANT ART CITED BY THE EXAMINER

23. The following prior art made of record and not relied upon is cited to establish the level of skill in the applicant's art and those arts considered reasonably pertinent to applicant's disclosure. See **MPEP 707.05(c)**.

24. The following references teach storing memory blocks wherein an even sector and an odd sector are stored in a single memory row location and explain reducing the size of a memory map.

U.S. PATENT NUMBER

US 6,757,800

US 2004/0199714

VIII. CLOSING COMMENTS

Conclusion

a. STATUS OF CLAIMS IN THE APPLICATION

25. The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**:

a(1) CLAIMS REJECTED IN THE APPLICATION

26. Per the instant office action, claims 1-20 have received a first action on the merits and are subject of a first action non-final.

b. DIRECTION OF FUTURE CORRESPONDENCES

27. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yaima Campos whose telephone number is (571) 272-1232. The examiner can normally be reached on Monday to Friday 8:30 AM to 5:00 PM.

IMPORTANT NOTE

28. If attempts to reach the above noted Examiner by telephone are unsuccessful, the Examiner's supervisor, Mr. Donald Sparks, can be reached at the following telephone number: Area Code (571) 272-4201.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

June 6, 2006

Yaima Campos
Examiner
Art Unit 2185

DONALD SPARKS
SUPERVISORY PATENT EXAMINER